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EXAMINER

PHAM, TAMMY T

ART UNIT

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/625,091	<b>Applicant(s)</b> TAKEMOTO, TAKAHIRO	
	<b>Examiner</b> TAMMY PHAM	<b>Art Unit</b> 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 28 October 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,3,11,13,21 and 25-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3,11,13,21 and 25-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### **Response to Amendment**

1. Claims 2, 7, 12, 17, have been cancelled. Claims 4-10, 14-16, 18-20, 22-24, have been withdrawn. Claim 28 has been added. Claims 1, 3, 11, 13, 21, 25-28, are considered below.

### **Response to Arguments**

2. Applicant's arguments filed 28 October 2010 have been fully considered but they are not persuasive.

#### **§ 103 Rejection**

3. **In regards to independent claims 1, 11, 21**, Applicant submits that the prior art fails to read upon the newly amended claims, because they fail to teach “*that ‘the polarity being oriented with respect to a vertical direction of the data lines’ (Remarks 13).*” This is not persuasive.

4. It is unclear as to what Applicant means by this. In particular, it is unclear what is mean in that the polarity is being orientated "with respect to" a vertical direction. Taking the broadest, reasonable interpretation, the prior art on record continues to read upon the claim limitations because since Moriyama teaches that the signal has a certain polarity (Fig. 3) and of data lines (Fig. 1, items X1-Xm). Due to the lack of language which describes how the polarity correlates to the data lines, the teachings of Moriyama continues to read upon the claim language as stated.

5. **In regards to independent claims 1, 11, 21,** Applicant submits that “Moriyama fails to disclose and teach the feature of the present invention that the relationship between the polarity of a horizontal period and the polarity of a next horizontal period, i.e., the same polarity along the vertical direction of the screen... *Therefore the resetting operation in the present invention is different form that of Moriyama (Remarks 13).*” This is not persuasive.

6. In particular, this argument is moot because this argument is based upon concepts which are not explicitly expressed in the claims. In particular, the claim language fails to explicitly claim how the resetting operations of Moriyama is distinguished from the current invention.

7. **In regards to independent claims 1, 11, 21,** Applicant submits that “in Moriyama, the writing operation is carried out by selecting the non-display data from the source driver circuit,, not by resetting the outputs of the source driver circuit (Remarks 14).” This is not persuasive.

8. In particular, this argument is moot because this argument is based upon concepts which are not explicitly expressed in the claims.

### **Claim Rejections - 35 USC § 102**

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 3, 11, 13, 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Moriyama et al. (US Patent No: 6,232,945 B1).

10. **In regards to independent claims 1, 11,** Moriyama teaches of an active-matrix addressing LCD device (Fig. 1, item 501) comprising:
  11. a panel including an active-matrix substrate (Fig. 1, item 101), an opposite substrate (Fig. 1, item 101), and a liquid crystal layer (Fig. 1, item 151) sandwiched by the active-matrix substrate (Fig. 1, item 101) and the opposite substrate (Fig. 1, item 101), the active-matrix substrate (Fig. 1, item 101) having data lines (Fig. 1, item X1-Xm), scanning lines (Fig. 1, item Y1-Yn) that intersect with the data lines (Fig. 1, item X1-Xm) at intersections, pixels (Fig. 1, item 151) arranged near the respective intersections, and TFTs (Fig. 1, item 121) arranged as switching elements (Fig. 1, item 121) for the respective pixels (Fig. 1, item 151);
  12. a source driver circuit (Fig. 1, item 291) for driving the data lines (Fig. 1, item X1-Xm);
  13. a gate driver circuit (Fig. 1, item 293) for driving the scanning lines (Fig. 1, item Y1—n);and
  14. a controller circuit (not shown) for controlling the source driver (Fig. 1, item 101) and the gate driver (Fig. 1, item 293),
  15. wherein a polarity of a data voltage (Fig. 18, item “Video Signal”) applied to each of the pixels (Fig. 1, item 151) by way of a corresponding one of the data lines (Fig. 1, item X1-Xm) and a corresponding one of the TFTs (Fig. 1, item 121) is inverted in every set of two or more horizontal synchronizing periods (Fig. 18, note that the “Video Signal” is inverted in at least every third horizontal synchronizing period) by the controller circuit (not shown);
  16. wherein the source driver (Fig. 1, item 291; Fig. 2) has a resetting means (Fig. 2) for resetting the data voltages outputted by the source driver circuit (Fig. 1, item 291; Fig. 2) in a

Art Unit: 2629

blanking period (Fig. 18, when the Reset Signal is ON) of each of the horizontal synchronizing periods of the set; and

17. wherein the resetting means (Fig. 2) performs its resetting operation (Fig. 2) with reference to a latch signal (Fig. 2, item “Reset”) supplied to the source driver circuit (Fig. 1, item 291; Fig. 2) by the controller circuit (not shown; column 6, lines 45-50; column 16, lines 45-50), the latch signal (Fig. 2, item “Reset”) being started between the end of the writing period (Fig. 3, item t2) and the end of the blanking period (Fig. 2, when Reset Signal is ON); and

18. wherein the resetting operation (Fig. 2) is completed before the writing period (Fig. 3, item t2) when the polarity of the data voltage (Fig. 18, item “Video Signal”) is not inverted (Fig. 18, item “Video Signal” is not inverted at time t2), the polarity being oriented with respect to a vertical direction of the data lines (Fig. 1, items X1-Xm), the writing period (Fig. 3, item t2) being a period (Fig. 3, item t2) where a data voltage (Fig. 3, item “video signal”) is applied, the resetting operation (Fig. 3, item “Reset”) comprising bringing values of all data voltages (Fig. 3, item “video signal”) closer to the middle point voltage between the positive (Fig. 3, positive values of “video signal”) and negative amplitudes (Fig. 3, negative values of “video signal”); and

19. wherein the data lines (Fig. 1, item X1-Xm) do not apply a subsequent data voltage (Fig. 18, item “Video Signal”) to each of the pixels (Fig. 1, item 151) in the blanking period (Fig. 2, when Reset Signal is ON); the subsequent data voltage (Fig. 18, item “Video Signal”) being a data voltage (Fig. 18, item “Video Signal”) that follows a previous data (Fig. 18, item “Video Signal”).

20. **In regards to independent claim 28**, in addition to the claim limitations as addressed above in claim 1, Moriyama further teaches of performing a resetting operation (Fig. 2) of resetting the data voltages (Fig. 18, item "Video Signal") outputted by the source driver circuit (Fig. 1, item 291; Fig. 2) in a blanking period (Fig. 2, when Reset Signal is ON) of each of the horizontal synchronizing periods of the set starting at an end of a writing period (Fig. 3, item t2), the resetting operation is completed when the data voltages (Fig. 18, item "Video Signal") are a middle point voltage during the blanking period (Fig. 2, when Reset Signal is ON).

21. **In regards to claims 3, 13**, Moriyama teaches that each of the data voltages (Fig. 18, item "Video Signal") alternately has a positive value or a negative value in the polarity inversion period; and

22. wherein the resetting means (Fig. 2) is controlled in such a way that each of the data voltages (Fig. 18, item "Video Signal") will reach a middle point value between the positive value (Fig. 18, positive value of "Video Signal") and the negative value (Fig. 18, negative value of "Video Signal") after the resetting operation (Fig. 2; Fig. 18, when the "Reset" pulse is ON) is completed (Fig. 18, column 16, lines 45-50).

### **Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

23. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriyama et al. (US Patent No: 6,232,945 B1) in view of Fukutofu et al. (U.S. Patent No.: 6,734,840 B2)

24. **In regards to claims 25-27**, Moriyama fails to teach that the data voltage applied to each of the pixels by way of the corresponding one of the data lines and the corresponding one of the TFTs is not inverted after each horizontal synchronizing period.

25. Fukutofu teaches that the polarity of the data voltage applied to each of the pixels by way of the corresponding one of the data lines and the corresponding one of the TFTs is not inverted after each horizontal synchronizing period (Fig. 3b, column 17, lines 19-24).

26. It would have been obvious to one with ordinary skill in the art at the time the invention was made to have the polarity not be inverted with every horizontal synchronizing period as taught by Fukutofu, with the display of Moriyama. This combination allows for a reduction or prevention of flickering and does not unnecessarily switch polarity patterns (Fukutofu, column 2, lines 46-54).

27. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriyama et al. (US Patent No: 6,232,945 B1) in view of Hirobumi (Japanese Publication No: 2001-249643).

28. **In regards to independent claim 21**, in addition the teachings of Moriyama above in claims 1, 11, Moriyama further teaches that the polarity of the data voltages (Fig. 18, item “Video Signal”) supplied by way of the data lines (Fig. 2, items X1-Xm) is alternately inverted in every set of the horizontal synchronizing periods (Fig. 18, item “One Horizontal Scanning Period”) and in every vertical synchronizing period (Fig. 21, item “Vertical Scanning Period”)



Art Unit: 2629

within every frame period (column 19, lines 10-15), thereby driving the device (Fig. 1, item 501).

29. Moriyama fails to specify that the polarity of the data voltages is inverted in every set of two horizontal synchronizing periods (the 2-H dot inversion method).

30. Hirobumi teaches that the polarity of the data voltages (Drawing 4, last waveform shown) is inverted in every set of two horizontal synchronizing periods (Drawing 4, item 2H) (the 2-H dot inversion method).

31. It would have been obvious to one with ordinary skill in the art at the time the invention was made to invert the data voltages every set of two horizontal synchronizing periods (the 2-H dot inversion method) as taught by Hirobumi with the display device of Moriyama because inverting the data voltage only one horizontal synchronizing period is insufficient in charging the LCD (Hirobumi, section [0010]).

**Conclusion**

32. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

33. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2629

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TP  
22 December 2010

*Tammy Pham*  
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Examiner, Art Unit 2629